Response Time of Embedded Networks: FlexRay and Time Triggered Ethernet

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A Time-Critical Task in Vehicle Embedded Network

• A Brake-by-Wire example



Emerging Networks: FlexRay/TTEthernet

Properties:

- Time-driven + event-driven traffic
- Distributed clock synchronization
- Fault-tolerance
- Response time important concern for time-critical apps: E.g. Brake-by-wire
- Our work: Computationally efficient method for computing worst-case response time and communication schedule

	CAN	FlexRay	ТТЕ			
Medium access	CSMA/CA	TDMA & FTDMA	TDMA & CSMA/CD			
Bandwidth	1 Mbit/s	10 (x2) Mbit/s	100 Mbit/s			
Frame size	14 – 8 bytes	264 – 254 bytes	1538 – 1500 bytes			
Topology	Bus	Bus, Star	Star, Line			
Composability	No	Yes	Yes			
Incremental update?	No	Yes	No			
Utilization in real setting	<40-50%	~30-50%, Max. 60-70%	~70%			
Image: State of the state o						



Overview of FlexRay

• Developed by an industry consortium, now ISO 10681 1&2: 2010 ECU ECU ECU ECU Channel A Dual channel bus Channel B Reserved bit Pavload preamble indicator Null frame indicator Sync frame indicator Startup frame indicator Frame format Payload Header Cycle CRC CRC CRC Frame ID Data 0 Data 1 Data n CRC length count 11 bits 0 ... 254 bytes 7 bits 6 bits 3 bytes 11 bits 11111 Trailer segment Header segment Payload segment Cycle *k*-1 Cycle *k* Cycle k+1MAC Static segment - TDMA Dynamic segment - FTDMA SW -NIT 2 3 5 2 3 4 5 6 7 8 9 10 11 12 4 6 1 $ID_{m1} = 2$ 3 5 6. $ID_{m2} = 4$ m^2 m1 m_{3} $ID_{m3} = 5$ 5 8 9 1 2 3 4 6 7 10 11 12 6/14/2012 322

Response Time Computation Problem

- Within DYN segment, higher priority msga delay lower priority ones
- For response time: Find worst case arrival sequence of higher priority msgs



• We formulate computation of β_m and δ_m as ILP (α_m and C_m are constants)



Our approach – Variables and Objective Functions

• Parameters (constants):

▶ Dom(m) = {m₁, m₂, ..., m_{p-1}}: Priority ordered messages of higher priority than m;
 ▶ Binary constant f_{ik} = 1 iff ID_i = ID_k;

- > T_i^{last} : Last minislot in which message *i* can be transmitted;
- $\succ \varphi_i$: extra minislots needed for transmission of message *i*;
- Variables:
 - > Binary decision variable $x_i^j = 1$ iff message *i* is transmitted in cycle *j*;
 - > Binary (auxiliary) variable $u_i^j = 1$ iff message *i* is not transmissible in cycle *j*.
- Objective functions:

> For computing β_m , Maximize number of nontransissible cycles:

Maximize
$$\sum_{j=0}^{U} u_p^j$$

> For computing δ_m , Maximize number of messages in the final cycle:

$$Maximize \sum_{i=1}^{p-1} x_i^{\{\beta_m+1\}} \times \varphi_i$$



Our approach – Constraints

- Non transmissibility condition (filled cycle condition) that defines u_i^j : $\left[u_i^j = 1\right] \Leftrightarrow \left[\sum_{k < i} x_k^j \times \varphi_k + ID_i > T_i^{last}\right] \vee \left[\sum_{k < i} x_k^j \times f_{ik} > 0\right], \forall i, j$
- A messages is transmitted only if it is transmissible: $x_i^j \le 1 - u_i^j, \forall i, j$
- Filled cycles for $m(=m_p)$ must be contiguous: $u_p^j \ge u_p^{\{j+1\}}, \forall j > 0$



Our approach – Constraints

• Arrival of messages must satisfy their minimum interarrival times:

$$\left[u_{i}^{j}=x_{i}^{j}=0\right]\wedge\left[x_{i}^{k}=1\right]\Rightarrow\left[\Delta_{i}^{\{j,k\}}>\left(\sum_{l=j}^{j+k}x_{l}^{l}-1\right)T_{i}\right],\forall i,j,k$$

where:

$$\Delta_i^{\{j,k\}} \coloneqq k \times T_{bus} + \left(\sum_{n < i} (x_n^k - x_n^j)\varphi_n\right) \times T_{MS}$$

is duration between j^{th} and $(j+k)^{\text{th}}$ cycles in which message *i* can be transmitted.

- Initial condition for cycle 0 (no transmission and transmissibility): $x_i^0 = u_i^0 = 0, \forall i$
- (Additional condition for 2nd objective function) Initial β_m cycles are filled: $u_p^j = 1, \forall 0 < j \leq \beta_m$



Validation over SAE Benchmark

• SAE benchmark: 7 ECUs exchanging 22 periodic & 31 aperiodic signals



• We consider three FlexRay configurations:

Parameter	Length Bus	Length ST segment	Length Minislot	Number Minislots
Config. C1	170	60	2	50
Config. C2	120	40	2	40
Config. C3	150	30	2	60

C1 & C2: some messages are unschedulable

➤ C3: all the messages are schedulable



Validation over SAE Benchmark



- Our formulation computes within 6 minutes for all msgs; Pop et al. failed to compute within an hour for certain messages (shown as -).
- For msgs Pop et al. is able to compute, it overestimates by as much as 30%



TTEthernet Protocol: Overview

- Defines Time-triggered (TT) service over Ethernet SAE AS6802
- Allows mixed time critical communication on a single physical network
 TT (Time-Triggered) frames: Period deterministic latency
 - RC (Rate-constrained) frames: Minimum interarrival time bounded latency
 - > BE (Best-Effort) frames: Standard Ethernet frames no transmission/delay guarantee
 - \succ Priority: TT \rightarrow RC \rightarrow BE





AFDX protocol for RC/TT Frames

Circuit Switching: Each frame sent from one node to a group of nodes over a virtual circuit (route) of links
 VL1, VL2
 VL2



- Parameters (constants):
 - \succ *s*(*i*): source node of frame *i*
 - > d(i): destination node of frame *i*
 - $\succ T_i$: minimum interarrival time of frame *i*
 - $\succ N_i$: Number of instances of frame *i* to be transmitted
 - $\succ C_i$: transmission time of frame *i*
 - $\succ X_{kk'}^{ij} = 1$ iff frames *i* and *j* share the link between nodes *k* and *k'*
 - $\succ Y_{kp}^{ij} = 1$ iff frames *i* and *j* both transit through node *k* at its input port p
 - $\succ Y_{kp}^i = 1$ iff frame *i* transits through node *k* at its input port *p*



TTEthernet – Variables/Objective Function

• Variables:

 $> a_k^{in}$: arrival time of *n*th instance of frame *i* at node *k*

• Objective function:

$$Maximize_n \left[a_{d(i)}^{in} - a_{s(i)}^{in}\right]$$



TTEthernet – Constraints for RC Frames

• Link is shared resource: Two frames arriving at the same switch port must be separated by at least the transmission time of the first arrived frame:

$$\left[a_k^{im} - a_k^{jn} \ge C_i Y_{kp}^{ij}\right] \vee \left[a_k^{jn} - a_k^{in} \ge C_j Y_{kp}^{ij}\right], \forall i, j, m, n, k, p$$

• Minimum interarrival time:

$$a_{s(i)}^{i(n+1)} - a_{s(i)}^{in} \ge T_i, \forall n, i$$

• First-Come First-Serve for frames:

$$[a_{k}^{im} - a_{k}^{jn}] \land [X_{kk'}^{ij} = 1] \Rightarrow [a_{k'}^{im} < a_{k'}^{jn}], \forall i, j, m, n, k, k'$$

• No idling of link when a frame is queued up for transmission:

$$\begin{bmatrix} a_k^{im} < a_k^{jn} \end{bmatrix} \wedge \begin{bmatrix} \left(a_k^{lo} \le a_k^{im} \right) \lor \left(a_k^{lo} \ge a_k^{jn} \right) \end{bmatrix} \wedge \begin{bmatrix} X_{kk'}^{ij} = 1 \end{bmatrix}$$

$$\wedge \begin{bmatrix} a_k^{jn} \le a_{k'}^{im} \end{bmatrix} \Rightarrow \begin{bmatrix} a_{k'}^{jn} = a_{k'}^{im} + C_j \end{bmatrix}, \forall i, j, k, k', m, n$$

$$\begin{bmatrix} a_k^{im} < a_k^{jn} \end{bmatrix} \wedge \begin{bmatrix} \left(a_k^{lo} \le a_k^{im} \right) \lor \left(a_k^{lo} \ge a_k^{jn} \right) \end{bmatrix} \wedge \begin{bmatrix} X_{kk'}^{ij} = 1 \end{bmatrix}$$

$$\wedge \begin{bmatrix} a_k^{jn} > a_{k'}^{im} \end{bmatrix} \Rightarrow \begin{bmatrix} a_{k'}^{in} = a_k^{in} + C_j \end{bmatrix}, \forall i, j, k, k', m, n$$



TTEthernet – Constraints for TT Frames

• Additional parameter:

> $P^{ij} = 1$ iff frame *i* higher priority than frame *j*

• (Modified constraint) Replace first-come-first-serve by highest-priority-first:

$$\begin{split} & [a_{k}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} \le a_{k'}^{im} - C_{i} \right] \wedge \\ & [P^{ij} > 0] \Rightarrow \left[a_{k'}^{im} = a_{k'}^{jn} + C_{i} \right], \forall i, j, k, k', m, n \end{split}$$

$$\end{split}$$

$$\begin{split} & [a_{k}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} \le a_{k'}^{im} - C_{i} \right] \wedge \\ & [P^{ij} \le 0] \Rightarrow \left[a_{k'}^{jn} = a_{k'}^{im} + C_{j} \right], \forall i, j, k, k', m, n \end{aligned}$$

$$\cr \begin{split} & [a_{k}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} > a_{k'}^{im} - C_{i} \right] \wedge \\ & [a_{k}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} > a_{k'}^{im} - C_{i} \right] \wedge \\ & [a_{k}^{im} < a_{k'}^{im}] \Rightarrow \left[a_{k'}^{jn} = a_{k'}^{im} + C_{j} \right], \forall i, j, k, k', m, n \end{aligned}$$

$$\cr \cr \begin{split} & [a_{k}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} > a_{k'}^{im} - C_{i} \right] \wedge \\ & [a_{k}^{im} < a_{k'}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} > a_{k'}^{im} \right] \Rightarrow \\ & [a_{k'}^{im} < a_{k}^{jn}] \wedge \left[\left(a_{k}^{lo} \le a_{k}^{im} \right) \vee \left(a_{k}^{lo} \ge a_{k}^{jn} \right) \right] \wedge \left[X_{kk'}^{ij} = 1 \right] \wedge \left[a_{k}^{jn} > a_{k'}^{im} \right] \Rightarrow \\ & [a_{k'}^{in} < a_{k'}^{jn} + C_{j} \right], \forall i, j, k, k', m, n \end{aligned}$$



Research Contributions

• FlexRay:

- ➤ A new ILP formulation for worst-case response time
- Our formulation: is exact and also non-iterative (so computationally more efficient) compared to literature
- SAE benchmark validations shows applicability to practical-sized problems
- ➢ To appear in IEEE Transactions on Automation Sc. & Engr.

• TTEthernet:

- ➤ A new MILP formulation for worst-case response time
- Implementation and evaluation ongoing

• Future direction:

- > A MILP-based framework for system level end-to-end timing analysis
- Integrate for system level assurance (eg, correctness of synchronous semantics under asynchronous execution)

